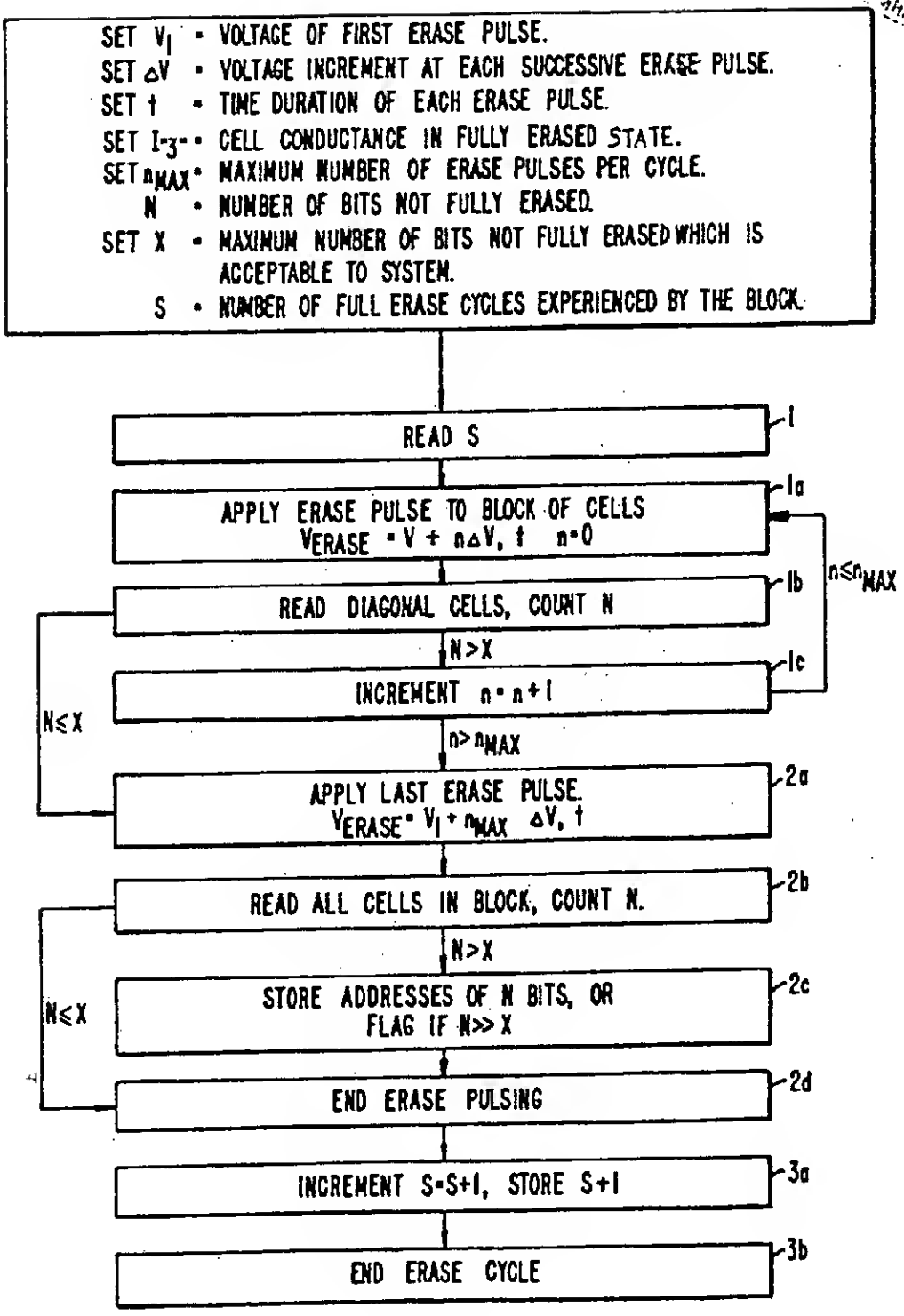
SET V_I - VOLTAGE OF FIRST ERASE PULSE.
SET ΔV - VOLTAGE INCREMENT AT EACH SUCCESSIVE ERASE PULSE.
SET t - TIME DURATION OF EACH ERASE PULSE.
SET I_{-3} - CELL CONDUCTANCE IN FULLY ERASED STATE.
SET n_{MAX} - MAXIMUM NUMBER OF ERASE PULSES PER CYCLE.
N - NUMBER OF BITS NOT FULLY ERASED.
SET X - MAXIMUM NUMBER OF BITS NOT FULLY ERASED WHICH IS ACCEPTABLE TO SYSTEM.
S - NUMBER OF FULL ERASE CYCLES EXPERIENCED BY THE BLOCK.
READ S
1
APPLY ERASE PULSE TO BLOCK OF CELLS
$V_{ERASE} = V + n\Delta V$, t n=0
1a
READ DIAGONAL CELLS, COUNT N
1b
N>X
INCREMENT n = n+1
1c
$n \leq n_{MAX}$
N≤X
$n > n_{MAX}$
APPLY LAST ERASE PULSE.
$V_{ERASE} = V_I + n_{MAX}$ ΔV, t
2a
READ ALL CELLS IN BLOCK, COUNT N.
2b
N>X
STORE ADDRESSES OF N BITS, OR FLAG IF N>> X
2c
N≤X
END ERASE PULSING
2d
INCREMENT S=S+1, STORE S+1
3a
END ERASE CYCLE
3b

FIGURE 9

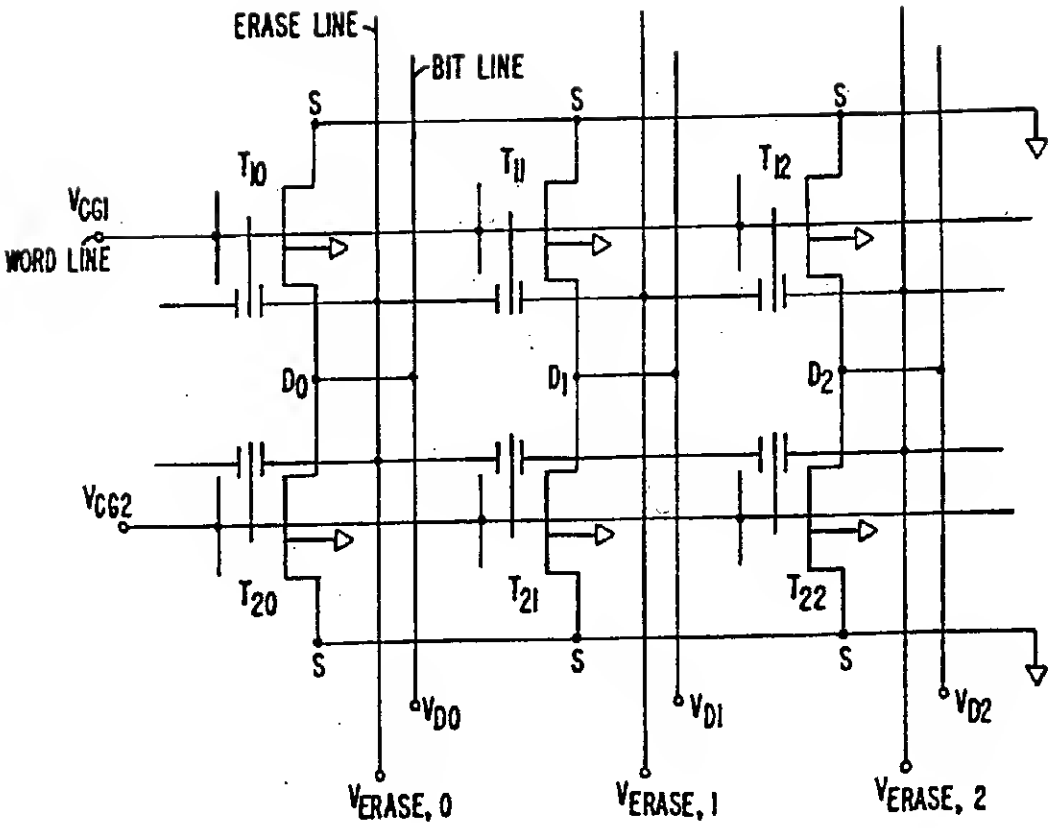
ERASE LINE
BIT LINE
S
S
S
T10
T11
T12
VCG1
WORD LINE
D0
D1
D2
VCG2
T20
T21
T22
S
S
S
VD0
VD1
VD2
VERASE, 0
VERASE, 1
VERASE, 2

FIGURE 10

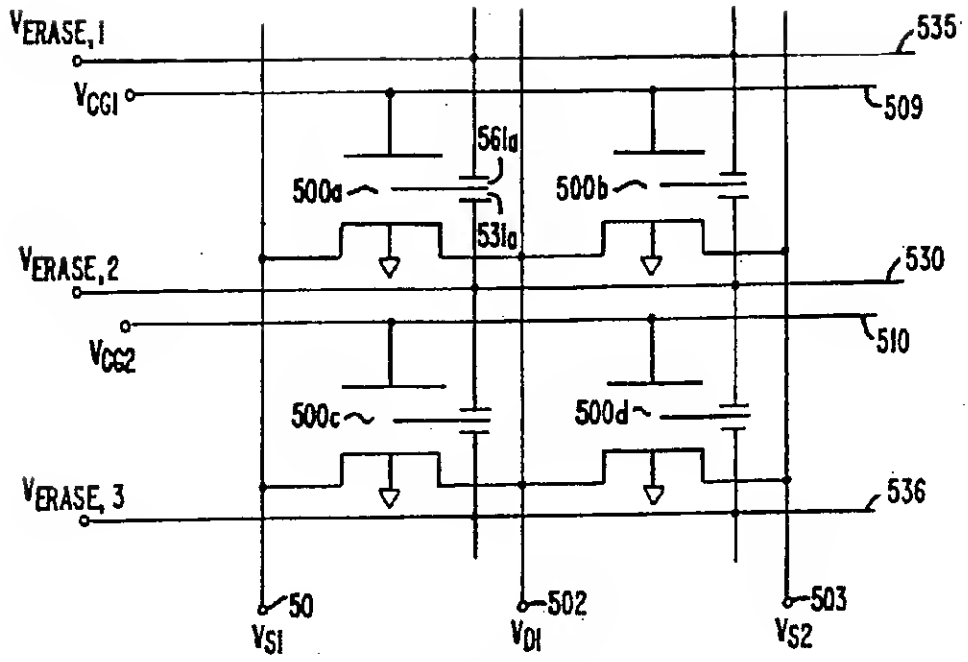
VERASE,1
VCG1
VERASE,2
VCG2
VERASE,3
561a
500a
531a
500b
500c
500d
535
509
530
510
536
50
VS1
502
VD1
503
VS2

FIGURE 11

TABLE I. ARRAY OF FIGURE 10

	V_{CG}			V_D			S			V_{ERASE}		
	SEL. CELL	UNSEL. CELL		SEL. CELL	UNSEL. CELL		SEL CELL	UNSEL. CELL		SEL. CELL	UNSEL. CELL	
		SAME ROW	SAME COL.		SAME ROW	SAME COL.		SAME ROW	SAME COL.		SAME ROW	SAME COL.
REAO	5V	5V	0V	1.5V	0V	1.5V	0V	0V	0V	0V	0V	0V
ERASE	0V	0V	0V	0V	0V	0V	0V	0V	0V	20V	20V (BLOCK	20V ERASE)
PROGRAM	12V	12V	0V	8V	0V	8V	0V	0V	0V	0V	0V	0V

FIGURE 12

TABLE II. VIRTUAL GROUND ARRAY OF FIGURE 11

	V_{CG}			V_D			S			V_{ERASE}		
	SEL. CELL	UNSEL. CELL		SEL. CELL	UNSEL. CELL		SEL. CELL	UNSEL. CELL		SEL. CELL	UNSEL. CELL	
		SAME ROW	SAME COL.		SAME ROW	SAME COL.		SAME ROW	SAME COL		SAME ROW	SAME COL.
READ	5V	5V	0V	1.5V	1.5V	1.5V	0V	1.5V	0V	0V	0V	0V
ERASE	0V	0V	0V	0V	0V	0V	0V	0V	0V	20V	20V (BLOCK	20V ERASE)
PROGRAM	12V	12V	0V	8V	FLOAT	8V	~0V	FLOAT	~0V	0V	0V	0V

FIGURE 13